EE231-Digital Logic Circuits (Required Course)

Code and Name: EE 231 Digital Logic Circuits
Credit Hours: 3 (Lecture: 3, Tutorial: 1)

Textbook:
- Digital Design, M. Morris Mano, Michael D. Ciletti, Fourth Edition, Prentice Hall, 2007.
Other References:
- Handouts in class that may help in addition to the main material.
- Roger L. Tokheim, *Schaum's Outline of Digital Principles*, Third edition

Course Description:
Number systems & codes; Boolean Algebra and logic gates; Karnaugh maps; Analysis and synthesis of combinational systems; Decoders, multiplexers, adders and subtractors, PLA's; Types of flip-flops; Memory concept; Counters and shift registers. Introduction to sequential circuit design.

Pre-requisites: MATH 105.
Co-requisites: None.

Course Learning Outcomes:
With relation to ABET Student Outcomes (SOs: 1-7)
1. Solve different logic circuits and execute calculations correctly. (1)
2. Solve problems based on formulas and techniques. (3)
3. Identify different techniques in digital logic circuits and combine them to solve problems related to higher order and in project. (3)
4. Use simulation tools for applications in electrical engineering. (6)
5. Develop solution for a design problem. (2)

Topics to be covered:

- Digital Systems. Binary Numbers. Number Base Conversions. Octal & Hexadecimal Numbers.
- Complements, Signed Binary Numbers, Binary Codes, Binary Logic.
- Basic Definitions. Axiomatic Definition of Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions. Canonical and Standard Forms.
- Other Logic Operations. Digital Logic Gates. Integrated Circuits.
- The Map Method. Four-Variable Map. Five-Variable Map. Product of Sums Simplification. Don't- Care Conditions. NAND and NOR Implementation.
- Exclusive-OR Function. Hardware Description Language (HDL). Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder-Subtractor. Decimal Adder. Binary Multiplier.
- Magnitude Comparator. Decoders. Encoders. Multiplexers. HDL for Combinational Circuits.
- Sequential Circuits. Latches. Flip-Flops. Analysis of Clocked Sequential Circuits.
- HDL for Sequential Circuits. State Reduction and Assignment. Design Procedure.
- Registers. Shift Registers. Ripple Counters.
- Synchronous Counters. Other Counters. HDL for Registers and Counters.
- Random Access Memory. Memory Decoding.
- Error Detection and Correction. Read-Only Memory. Programmable Logic Array.
- Programmable Array Logic. Sequential Programmable Devices.

Grading Policy:
The grading for the course are 60% coursework and 40% Final Exam. The coursework consists of two Midterm Exams, where each midterm exam is worth 20%. It also includes quizzes, homework, and projects for the remaining 20% that is modified by the course instructor.