2023
TP-153

Course Specification
(Bachelor)

Course Title:	Digital Logic Circuits
Course Code:	EE1331
Program:	Electrical Engineering
Department:	Electrical Engineering
College:	College of Engineering
Institution:	Imam Mohammad Ibn Saud Islamic University
Version:	V3
Last Revision Date:	10-10-2024

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (3)					
2. Course type					
A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☒ Required		☐Elective		
3. Level/year at which this course is offered: (3rd level, 2nd year)					
4. Course general Description:					
Number systems & codes; Boolean Algebra and logic gates; Karnaugh maps; Analysis and synthesis of combinational systems; Decoders, multiplexers, adders and subtractors, PLA's; Types of flip-flops; Memory concept; Counters and shift registers. Introduction to sequential circuit design.					
5. Pre-requirements for this course (if any)**:**					
MATH1115					
6. Co-requisites for this course (if any)**:**					
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7. Course Main Objective(s):					
1. Providing students with the fundamental technical knowledge and skills to be able to recognize, analyze and solve basic digital systems and binary number arithmetic 2. To understand the basic vocabulary and brief foundation in Boolean algebra. 3. To introduce the students to a design methodology for describing and designing large complex digital systems. 4. To understand the integrated circuit (IC) and the digital logic families and analyze their operation.					

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	60	100%
2	E-learning	-	-
3	Hybrid • Traditional classroom • E-learning	-	-
4	Distance learning	-	-

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	45
2.	**Laboratory/Studio**	-
3.	**Field**	-
4.	**Tutorial**	15
5.	**Others (specify)**	-
Total		60

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
K1	Students will be able to solve different logic circuits and execute calculations correctly.	1.3	Delivering Lectures Solve problems in groups during tutorial	Quizzes in class Midterm exam Final exam
K1	Students will be able to solve problems based on formulas and techniques.	1.2	Delivering Lectures Solve problems in groups during tutorial	Quizzes in class Midterm exam Final exam
K2	Students will be able to identify different techniques in digital logic circuits and combine them to solve problems related to higher order and in a project	7.1	Delivering Lectures Solve problems in groups during tutorial	Quizzes in class Midterm exam Final exam
2.0	**Skills**			
S1	Students will be able to develop a solution for a design problem	2.2	Delivering Lectures Solve problems in groups during tutorial	Quizzes in class Midterm exam Final exam
3.0	**Values, autonomy, and responsibility**			
V1	Students will be able to identify different techniques in digital logic circuits and combine them to solve	3.1	Delivering Lectures Solve problems in groups during tutorial	Quizzes in class Midterm exam Final exam

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
	problems related to higher order and in a project			

C. Course Content

No	List of Topics	Contact Hours
1	Digital Systems. Binary Numbers. Number Base Conversions. Octal & Hexadecimal Numbers.	6
2	Complements, Signed Binary Numbers, Binary Codes, Binary Logic	6
3	Basic Definitions. Axiomatic Definition of Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates. Integrated Circuits	6
4	The Map Method. Four-Variable Map. Five-Variable Map. Product of Sums Simplification. Don't- Care Conditions. NAND and NOR Implementation	6
5	Exclusive-OR Function. Combinational Circuits. Analysis Procedure. Binary Adder-Subtractor. Decimal Adder. Binary Multiplier.	6
6	Magnitude Comparator. Decoders. Encoders. Multiplexers. HDL for Combinational Circuits.	6
7	Sequential Circuits. Latches. Flip-Flops. Analysis of Clocked Sequential Circuits.	6
8	Registers. Shift Registers. Ripple Counters	6
9	HDL for Sequential Circuits. State Reduction and Assignment. Design Procedure	6
10	Hardware Description Language (HDL). Implementation of simple logic gates and combinational circuits. HDL for sequential circuits.	6
Total		**60**

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Midterm 1	7^{th} week	20%
2.	Midterm 2	13^{th} week	20%
3.	Homework + Quizzes	During the Course	20%
4.	Final Exam	Final Exam week	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	Digital Design, M. Morris Mano, Michael D. Ciletti, Prentice Hall, 5th edition 2013
Supportive References	1. Handouts in class that may help in addition to the main material. 2. M. Morris Mano, Charles R. Kime, Tom Martin, Logic and Computer Design Fundamentals, 5th Edition, Pearson Publishers. 3. Thomas L. Floyd, Digital Fundamentals, 11th Edition, Pearson Publishers.
Electronic Materials	Computer animations and online resources supplied by the instructor.
Other Learning Materials	Different Online sites.

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	One classroom: fits up to 25 students with white board.
Technology equipment (projector, smart board, software)	A laptop computer connected to a projector to display PowerPoint presentations
Other equipment (depending on the nature of the specialty)	N/A

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of teaching	**Students**	**Indirect**
Effectiveness of Students assessment	**Students**	**Indirect**
Quality of learning resources	**Relevant Focus Group**	**Indirect**
The extent to which CLOs have been achieved	**Dept. Quality Committee**	**Direct**
Other		

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	