2023
TP-153

Course Specification
(Bachelor)

Course Title:	Digital Logic Circuit Lab
Course Code:	EE1333
Program:	Electrical Engineering
Department:	Electrical Engineering
College:	College of Engineering
Institution:	Imam Mohammad Ibn Saud Islamic University
Version:	V5
Last Revision Date:	01-01-2025

Table of Contents

A. General information about the course:

1. Course Identification

1. Credit hours: (1)					
2. Course type					
A.	☐University	☐College	☒ Department	☐Track	☐Others
B.	☒ Required		☐Elective		
3. Level/year at which this course is offered: (4th level, 2nd year)					
4. Course general Description:					
Hands-on experience to design, construct and analyze different logic circuits. Student will construct logic circuits using integrated circuit (IC), logic breadboard, LEDs, power supply and other basic components. Both combinational and sequential logic circuits will be given in experiments. Design and analyze various digital circuits involving logic gates, multiplexers, decoders, flip-flops, counters and registers is included. Simulation using hardware descriptive language (HDL) such as Verilog will be covered.					
5. Pre-requirements for this course (if any)**:**					
GE1101, EE1331, EE1201					
6. Co-requisites for this course (if any)**:**					
7. Course Main Objective(s):					
The main purpose is to study the following topics experimentally: Simplification of Logic equations, Design and Analysis of Combinational Circuits such as adders, subtractors, code convertors, multiplexers, demultiplexers, coders , decoders etc., Design and analysis of Sequential Circuits such as counters , shift registers etc.					

2. Teaching mode (mark all that apply)

No	Mode of Instruction	Contact Hours	Percentage
1	Traditional classroom	30	100%
2	E-learning	-	-
3	Hybrid • Traditional classroom • E-learning	-	-
4	Distance learning	-	-

3. Contact Hours (based on the academic semester)

No	Activity	Contact Hours
1.	**Lectures**	-
2.	**Laboratory/Studio**	30
3.	**Field**	-
4.	**Tutorial**	-
5.	**Others (specify)**	-
Total		30

B. Course Learning Outcomes (CLOs), Teaching Strategies and Assessment Methods

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
1.0	**Knowledge and understanding**			
K1	List and recall Basic Gates and their Truth Tables, Flip Flops and their Truth Table, Block diagrams of some standard circuits Boolean algebra.	**1.1**	Talk & Chalk, Demonstration	Quizzes in class Midterm exam Final exam
K2	Design and demonstrate different sequential Circuits experimentally	**7.2**	Talk & Chalk, Demonstration	Quizzes in class Midterm exam Final exam
2.0	**Skills**			
S1	Design and demonstrate different Combinational Circuits experimentally	**2.2**	Talk & Chalk, Demonstration	Quizzes in class Midterm exam Final exam
S2	Adapt lab procedure.	**6.1**	Talk & Chalk, Demonstration	Quizzes in class Midterm exam Final exam
S2	Analyze and demonstrate different	**6.2**	Talk & Chalk, Demonstration	Quizzes in class Midterm exam

Code	Course Learning Outcomes	Code of CLOs aligned with program	Teaching Strategies	Assessment Methods
	Combinational and sequential Circuits experimentally			Final exam
3.0	**Values, autonomy, and responsibility**			
V1	Document data in report.	**3.2**	Demonstration on how to prepare report using computer	Lab Report

C. Course Content

No	List of Topics	Contact Hours
1	Digital logic circuit trainer introduction	2
2	Boolean algebra and functions	2
3	Combinational circuits	2
4	Code converters: Binary to Gray, BCD to Excess-3	2
5	Code converters: Binary to BCD, BCD to 7-segment display	2
6	Multiplexers: design and applications	2
7	Decoders: functional verification and their use	2
8	Half adder and full adder	2
9	Half and full subtractor	2
10	Latches – level sensitive storage elements	2
11	Flip-flops – Edge triggered devices	2
12	Up counter design and timing analysis	2
13	Down counter and Mod-N	2
14	Shift registers – serial-in serial-out and serial-in parallel-out	2
15	Shift registers – parallel-in serial-out and parallel-in parallel-out	2
15	Mid and Final Exam	4
Total		**34**

D. Students Assessment Activities

No	Assessment Activities *	Assessment timing (in week no)	Percentage of Total Assessment Score
1.	Reports	Every week	20%
2.	PreLab Quiz	Weekly	10%
3.	Quiz	10th Week	10%
4.	Final Exam	Final Exam week	40%

*Assessment Activities (i.e., Written test, oral test, oral presentation, group project, essay, etc.).

E. Learning Resources and Facilities

1. References and Learning Resources

Essential References	Lab manual Given by University M. Morris Mano, Digital Design Third Edition, Pearson Education Limited.
Supportive References	Given by teacher at different time during the course
Electronic Materials	Computer animations supplied by the instructor.
Other Learning Materials	Using Softwares is Encouraged for Simulation Purpose other than that of Lab.

2. Required Facilities and equipment

Items	Resources
facilities (Classrooms, laboratories, exhibition rooms, simulation rooms, etc.)	SR 137 in Lab Room with 10 Students per Section
Technology equipment (projector, smart board, software)	Lab Equipment: Digital Logic board with patch chords, Blackboard LMS software, data-show, and white board.
Other equipment (depending on the nature of the specialty)	Provided in the lab.

F. Assessment of Course Quality

Assessment Areas/Issues	Assessor	Assessment Methods
Effectiveness of teaching	**Students**	**Indirect**
Effectiveness of Students assessment	**Students**	**Indirect**
Quality of learning resources	**Relevant Focus Group**	**Indirect**
The extent to which CLOs have been achieved	**Dept. Quality Committee**	**Direct**
Other		

Assessors (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)

Assessment Methods (Direct, Indirect)

G. Specification Approval

COUNCIL /COMMITTEE	
REFERENCE NO.	
DATE	